REWORKABLE EDGEBOND APPLIED WAFER-LEVEL CHIP-SCALE PACKAGE (WLCSP) THERMAL CYCLING PERFORMANCE ENHANCEMENT AT ELEVATED TEMPERATURE

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ABSTRACT
This paper presents data showing that localized distribution of recrystallized grains is an accurate indicator of solder joint life-cycle degradation and enhancement. Monitoring the distribution is proposed as a new analytical approach. The correlation between an elevated temperature environment and thermal cycling induced crack propagation, in a series of cross section analyses, on reworkable edgebond material applied wafer level chip scale package (WLCSP) components was conducted. The printed circuit board was designed to provide elevated temperature during thermal cycling by an embedded heating element inside the PCB. The localized heating of the WLCSP, to simulate an active component, degrades life cycles due to a higher creep rate, which negatively impacted the crack propagation. The application of a reworkable edgebond material enhanced thermal cycling fatigue performance. Use of a reworkable edgebond adhesive enhanced life cycles for both normal temperature and elevated temperature thermal cycling. Monitoring local distribution of recrystallized grains is a promising approach to collecting predictive lifecycle data. This paper will discuss the overall performance of the reworkable edgebond, which provided a good stability enhancement to the WLCSP structure under thermal cycling at elevated temperature environment.

Key words: Edgebond, WLCSP, thermal cycling, elevated temperature test, recrystallization

INTRODUCTION
Each electric component of the vast variety of device packaging types, have their own life cycle to failure in a wide spread thermal cycling performance. The selected components, as shown in Figure 1, were tested at the same testing thermal cycling condition, 0°C to 100°C with a 10min dwell time, but show a wide span of performance. Addition to that, the board thickness condition variation added a more complex performance chart. [1]

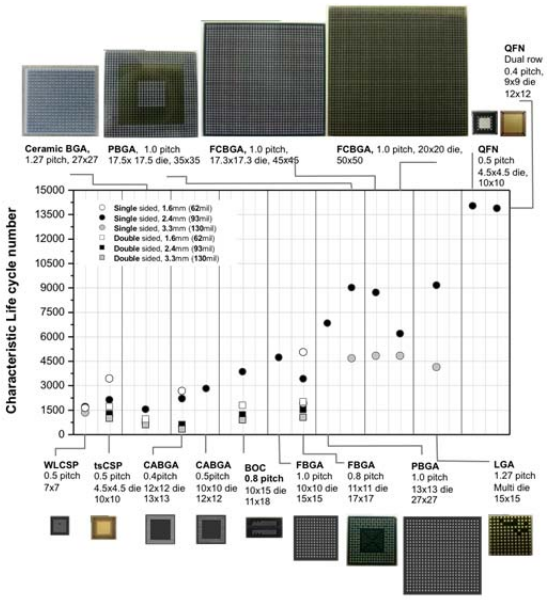

Figure 1. Characteristic lifecycle per various package types.

The source of the variations are in general based on die size, substrate thickness, solder alloy composition, surface finish and ball pitch etc. It is well known that wafer level chip scale packages (WLCSP) are relatively shorter in characteristic lifecycle time subject to thermal cycling due to the higher CTE mismatch with the PCB. [2,3] But given the fact that WLCSPs are more and more implemented into the industry sector via internet of things (IoT) and industry automation acceleration, it is important to enhance the lifecycle time for these WLCSP for higher reliability. Improving the thermal cycling performance of WLCSP can be achieved by various approaches, one of them is the

strengthening of the solder joint by applying a new solder alloy composition. Another approach is the enhancement of the total package, which is the use of underfill material. But even if it is a mature technology, the underfill process at the BGA board level component has a few challenges associated with no-clean flux residue, which can negatively impact the interface between the underfill material and the board interface. The re-workability of large underfilled components is also a factor, which needs to be thoroughly considered. An alternative approach is a localized enhancement using edge-bond materials. The outer array solder joints experience most of the damage accumulation during thermal cycling, thus an enhancement targeting those solder joints can result in a higher thermal cycling performance. As shown in Figure 2, each solder joint accumulate defects constantly and experience a degradation during thermal cycling. The mechanism, leading to crack initiation and propagation during thermal cycling is by sub-grain boundary development, and can be observed as a general damage accumulation mechanism in various solder joints. [4,5] Figure 2(a) shows a Package on package (PoP) component cross section during thermal cycling, where the corner joint at as-assembled state show no sign of grain refinement. But after thermal cycling, a grain refined/recrystallized regions were revealed locally. The example in Figure 2(b) also shows the same development of localized grain refinement/recrystallized region after thermal cycling. In earlier publications the degradation and deformation mechanism were studied and showed the microstructure evolution associated with the thermal cycling induced damage accumulation. [1,6] A wide distribution of recrystallized grains after thermally cycled WLCSP can be seen in most of the solder joints, with the associated crack propagation. Using this methodology, observing the grain structure evolution during or after thermal cycling, can indicate the stressed/strained damage solder joints and give a more detailed information whether the joints are at high risk location or not. [7-9] Implementing the edgebond on WLCSP components is expected to alter the shear mode and degradation mechanism due to the mitigation of the corner location strain, which usually caused by large CTE mismatch. To enable a more detailed and in-depth analysis,

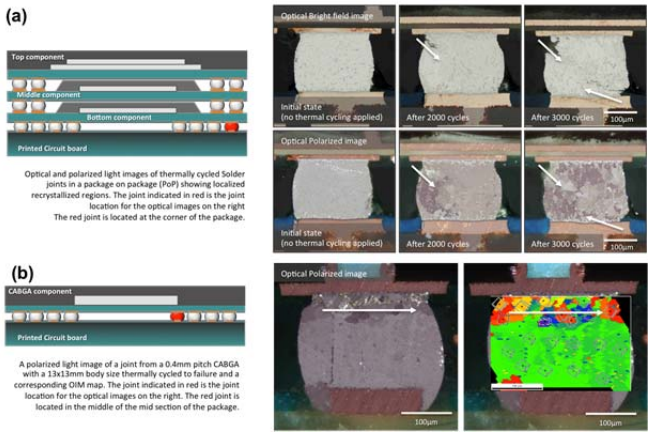

Figure 2. Microstructure signatures

the grain structure development inside the solder joints were observed and signature structures are identified to understand the behavior of the interconnects on edgebond applied and thermal cycled components. Monitoring and following the grain structure evolution, one might be able to assess the failure mechanism associated with the critical solder joint location in the given package, used as a damage accumulation indicator. The higher rate of grain refinement and recrystallization indicated that, which solder joint is the most damaged joint during thermal cycling, which ultimately indicates, which joint needs enhancement. Another factor considered in this paper and evaluation process is the function temperature of the device. Since WLCSP packages are directly exposed to air, the temperature of the package can directly impact the edge-bond materials attached to the device. Thus a test at an elevated temperature is valuable to consider. To achieve the elevated temperature environment, a heating layer was embedded in the PCB to increase the overall temperature to a constant temperature of 50°C. The paper presented here is on localized solder enhancement using edge-bond materials to improve the thermal cycling performance at normal temperature and elevated temperature environment.

EXPERIMENTAL PROCEDURE

8x8mm with 0.4mm pitch, 250µm solder ball diameter WLCSP components were used in this study. A schematic diagram of the WLCSP sample configuration and the picture of the top view of the edgebond applied and not applied WLCSP components are shown in Figure 3. Solder balls attached to the packages were all composed of Sn-4.0Ag-0.5Cu (wt%) (SAC405). The parts were board-assembled on 93mil high glass transition temperature (T_g), FR4-printed circuit boards with OSP surface finishes with a thermal profile of peak temperatures of 240 °C, 60 seconds above the liquidus temperature. All components were

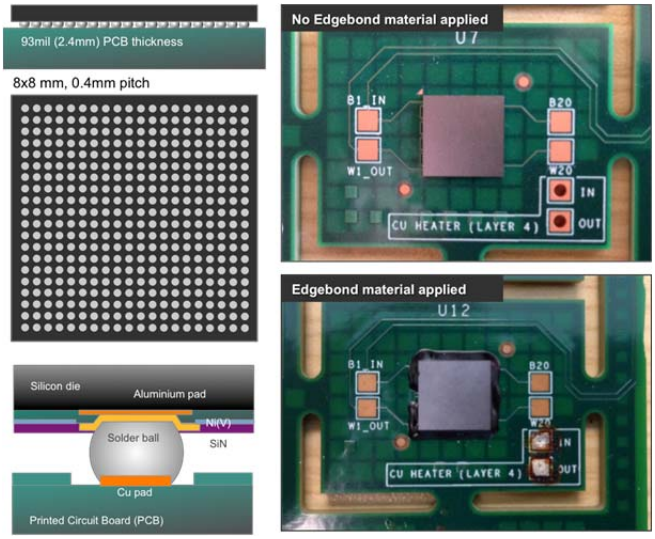

Figure 3. Test vehicle

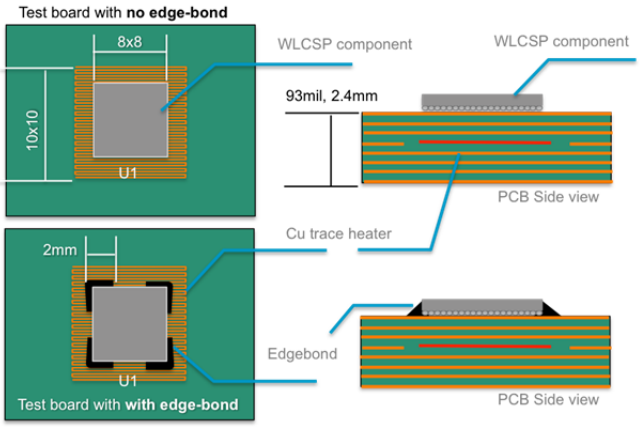

Figure 4. Embedded heating element PCB schematics

assembled with SAC305 solder paste. For edge-bond process, commercially available edge-bond adhesive were selected. A high T_g 130°C and low CTE 30ppm/°C reworkable edge-bond material was provided and processed by Zymet. To prevent voiding due to moisture releasing from PCB material in curing cycle, test boards are pre-baked for 4 hours at 125°C. The edge-bond adhesives were dispensed at room temperature using a pneumatic, hand-held dispenser. The board was then cured at 150°C for 30 minutes. The edegbond material covered three full edges and one side-edge partially opened as shown in Figure 3. For thermal cycling, samples were cycled from 0 to 100 °C at a ramp rate of 10 °C per minute with 10 minutes of dwell time. A continuous resistivity measurement using a data logger was applied for each channel in situ monitoring during the test. The failure criterion in this study was based on the JESD22-A104D standard [10], a 20% increase of the peak resistivity for continuous five cycles relative to the initial value. To achieve an elevated temperature environment additional to the thermal cycling temperature, a heating element at the fourth layer of the PCB was implemented in an eight layer PCB. The heater was able to bring up the localized temperature under the component to 80°C with a nominal electric current. The elevated temperature for this study was fixed to 50°C. Figure 4 shows the schematic drawings of the heater cover area and the test sample configurations. The heater covered the area of 10x10mm below the component and the test temperature of 50 °C modified the thermal cycling temperature profile from 0 °C~100 °C to a thermal cycling profile of ~25 °C to 125°C. An external power source provide a current of ~0.85A which increased the temperature of the component location to 50°C. The input current was calibrated to maintain the constant temperature for each component location. The thermal cycling results for each condition were plotted as Weibull distribution plots. Cross-sectional analysis using optical microscope with bright light and polarized light were applied to observe the evolution of the microstructures and the locations of the solder joint cracks.

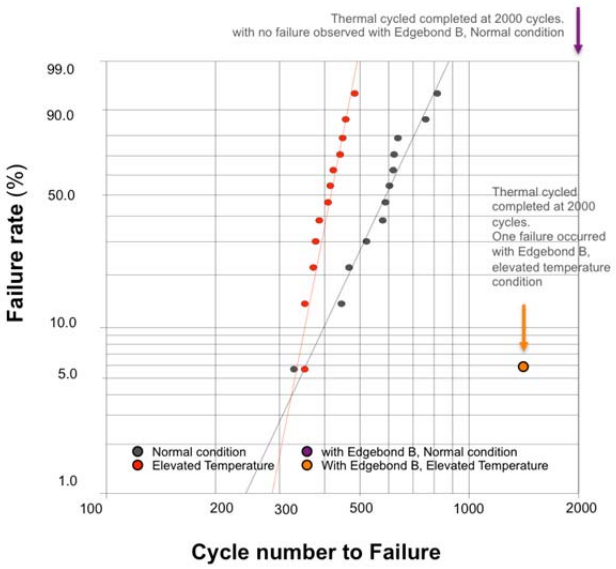

Figure 5. Thermal cycling result Weibull plot

RESULTS AND DISCUSSION

The thermal cycling results are shown in Figure 5. All four test results are accumulated in the Weibull plot; no-edgebond applied normal and elevated temperature thermal cycling and edgebond applied normal and elevated temperature thermal cycling applied conditions. Both no edgebond applied normal and elevated temperature thermal cycled samples show a relatively lower cycle to failure

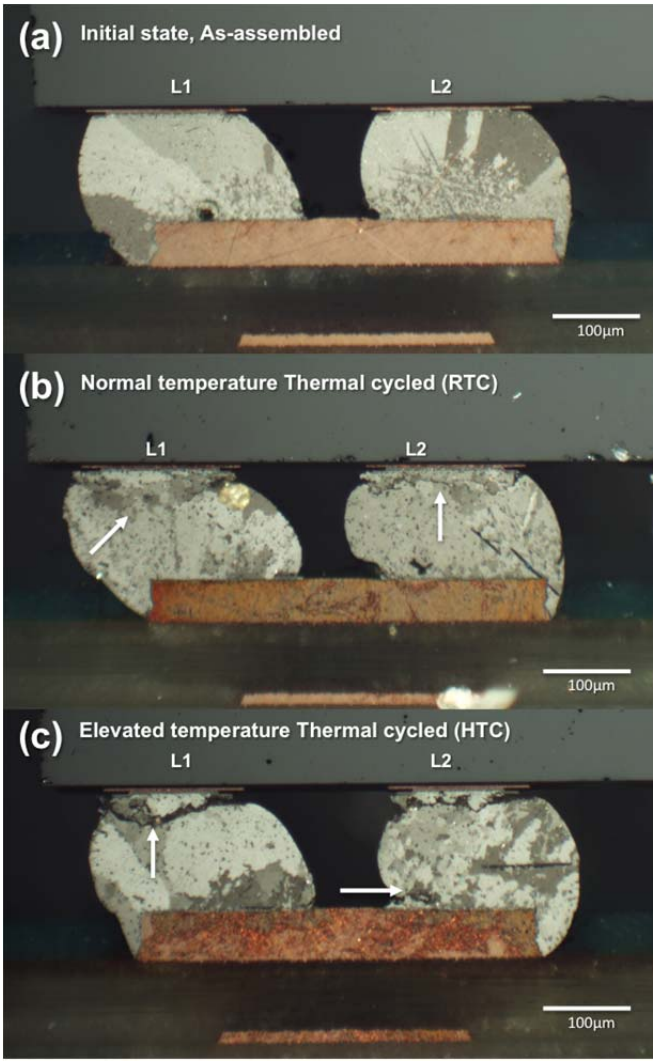

Figure 6. Optical polarized images of (a) as-assembled, (b) normal temperature TC and (c) elevated temperature TC

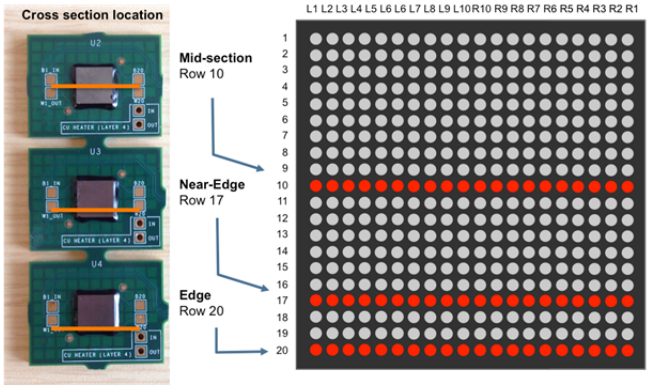

Figure 7. Cross section location

distribution. The edgebond applied samples, showed only one failure until 2000cycles, where the test was stopped. The single failure for the edgebond-applied sample was a sample tested at elevated thermal cycling. Given the fact that no edgebond applied samples first failure was detected at 355 cycles, it is already a ~500% increase of performance with the edgebond material applied. The comparison between normal and elevated temperature thermal cycling, the lifecycle number degraded from 638 cycles characteristic cycle to 430 cycles, a 33% degradation of life cycle numbers. But the first failure cycle numbers were similar with actually an earlier first failure cycle number for the normal temperature thermal cycling with 331 cycles. It is somewhat expected to have a degraded performance for an elevated test condition since the temperature cycle range increased from 0 to 100°C to 25 to 125°C. An overall higher creep rate is expected resulted in faster crack propagation rate. The faster degradation during thermal cycling for the elevated temperature tested samples can be seen in the grain structure evolution, shown in Figure 6. Two solder joints from each sample condition, joint corners, as-assembled, no edgebond applied with normal and elevated thermal cycling are presented. The as-assembled solder joints (Figure 6(a)) show the normal grain structure with single, dual and beach ball grain structure with localized interlace structure at the interface region. But after thermal cycling both normal and elevated temperature thermal cycled samples show crack developed at the package side interface. The difference between the normal and elevated temperature thermal cycled samples, is the recrystallization region near the crack path. For the normal thermal cycled samples in Figure 6(b), the recrystallized region appeared near the crack path, as indicated by an arrow. But the elevated temperature thermal cycled joints show a relatively smaller region of recrystallized region near the crack. One more difference between these two conditions is the overall fine grain structure development. The elevated temperature thermal cycling in Figure 6(c) shows an overall transition from single/dual grain structure to a more refined smaller grain distribution, but the normal thermal cycled sample show a relatively more localized grain refinement, limited to the crack propagation path. For the edgebond applied samples, the failure was not identified until the test was stopped, but partial crack development was observed after 2000cycles. Figure 7 shows the cross section row location per sample after thermal cycling at elevated temperature. The edge row, the 17th row inside the component and the mid section of the component were subjected for cross section and the images of the entire row for each condition are shown in Figure 8. Figure 8(a) shows the polarized images for each row cross section for the initial, as-assembled state solder joints, Mid-section, near edge section (17th row) and the edge row cross section images. It is observed that the edge row joints developed a grain recrystallization structure after thermal cycling without developing a full or partial crack. The recrystallization/grain refinement distribution maps for each

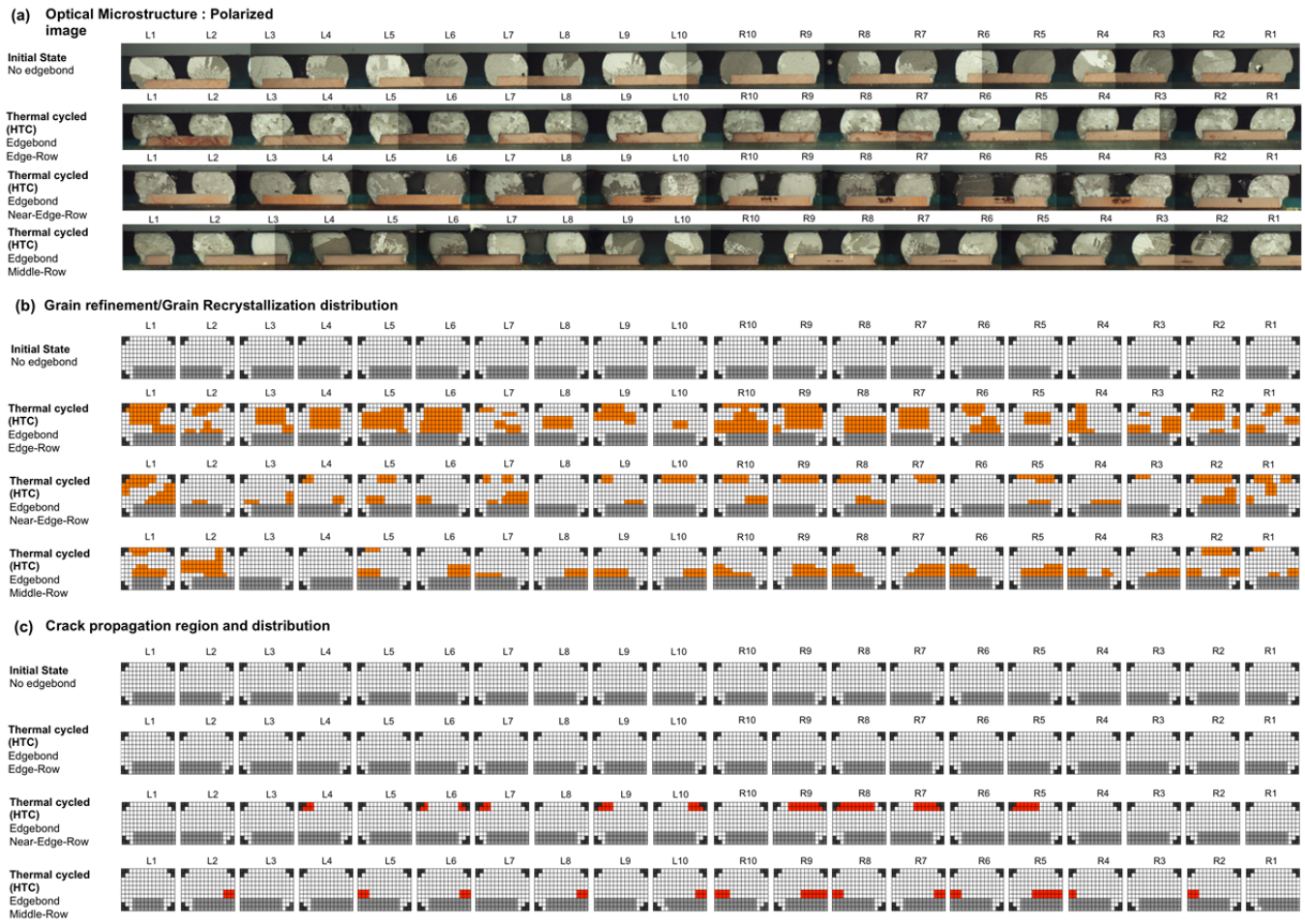

Figure 8. Grain structure distribution chart. (a) Optical polarized image, (b) Recrystallization region distribution and (c) Crack propagation distribution; for as-assembled, Edgebond applied component after thermal cycling cross section at mid section, near edge and edge row.

associated joints are shown in Figure 8(b). Where the edge-row joints do not show any indication of crack propagation (Figure 8(c)). Compared to the edge-row joints, the near-edge row joints (at the 17th row) begin to show partial crack development at the package side interface, which is associated with the recrystallized region indicated in Figure 8(b). But it is interesting to see that the crack location shifted to the board side interface region once the cross section moves into the mid-section of the component. This observation indicates that the edgebond material provide stability at the edge row and shift the deformation and damage accumulation location into the component interior located solder joint. The damage accumulation indications via grain refinement observation tells us that the defect accumulation and deformation occurred at the board side interface for the mid-section solder joints. But compared to the mid section joints, the near edge row (row 17) solder joints experienced a deformation at the package side interface. By utilizing the grain structure distribution, the mostly damages area can be identified for further understanding the degradation mechanism for given component structure.

CONCLUSION

This paper presents data showing that localized distribution of recrystallized grains is an accurate indicator of solder joint life-cycle degradation and enhancement. Monitoring the distribution is proposed as a new analytical approach. The correlation between an elevated temperature environment and thermal cycling induced crack propagation, in a series of cross section analyses, on reworkable edgebond material applied wafer level chip scale package (WLCSP) components was conducted. The printed circuit board was designed to provide elevated temperature during thermal cycling by an embedded heating element inside the PCB. The localized heating of the WLCSP, to simulate an active component, degrades life-cycle due to a higher creep rate. This higher creep rate negatively impacted the crack propagation. The application of a reworkable edgebond material enhanced thermal cycling fatigue performance. The edgebond material provide stability at the edge row and shift the deformation and damage accumulation location into the component interior located solder joint. The damage accumulation indications via grain refinement observation tell us that where the defect accumulation and deformation occurred. Monitoring local

distribution of recrystallized grains is a promising approach to collecting predictive life-cycle data.

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