MULTI-AXIS LOADING EFFECT ON EDGEBOND AND CORNERFILLED WLCSP THERMAL CYCLING PERFORMANCE

Andy Hsiao and Tae-Kyu Lee
Portland State University
OR, USA
taeklee@pdx.edu

Edward Ibe and Karl Loh
Zymet
NJ, USA

ABSTRACT
Various external load conditions affecting components on electronic devices and modules are constant factors, which need to be considered for the component long-term reliability. Recently, to enhance the high stress component thermo-mechanical cycling performance, various types and configuration using edgebond and cornerfill technology are introduced and tested. These applications induce a multi-axis loading condition, which alter the degradation mechanism and failure location during thermal cycling, which need closer investigation. In this study, high stress 12x12mm^2 wafer level chip scale packages (WLCSP) were selected and subject to thermal cycling with full-edgebond, dot-edgebond and cornerfill adhesive, which improves the characteristic lifecycle numbers base on the configurations, but altered the failure location due to different stress conditions. The -40 to 125^{o}C thermal cycling profile revealed localized degradation per configuration during thermal cycling, showed a shift of the crack propagation path, based on full-edgebond, dot-edgebond and cornerfill adhesive sample conditions. Through these series of observation, the interconnect thermal cycling degradation mechanisms are able to be explained. The correlation between the stress condition and microstructure are presented and discussed based on EBSD analysis.

Key words: Edgebond, Dot-edgebond, Cornerfill, thermal cycling, recrystallization.

INTRODUCTION
It is well known that wafer level chip scale packages (WLCSP) are presenting shorter characteristic lifecycle numbers subject to thermal cycling due to the higher CTE mismatch with the PCB. [1,2] But the industry sector on internet of things (IoT) and industry automation are in high speed in transformation where WLCSP are playing a crucial role due to its form factor and simple structure, which obviously brings an economical benefit. But at the sametime it is important to enhance the lifecycle time for these WLCSP for higher reliability since the automation and controllability is crucial to the safety of the electronic system. With higher function per component need, increasing in WLCSP body size is a constant challenge, since larger WLCSP have higher thermal coefficient mismatch resulting in a higher stress at the corner interconnects between the component and PCB. [3] As shown in Figure 1, larger WLCSP body size components show significantly lower thermal cycling performance. The selected components in Figure 1, were tested at the same testing thermal cycling condition, 0^{o}C to 100^{o}C with a 10min dwell time on 93mil thickness PCB and were all with SAC305 solder balls and 0.4mm pitch. Thus having a WLCSP larger than 8x8mm in body size will have a high chance to demonstrate a thermal cycling performance less than ~300cycles, which will be a limitation factor for WLCSP for long-term reliability application. Overcoming this challenge and improving the thermal cycling performance of WLCSP can be achieved by a few approaches. One of them is the strengthening of the solder joint material itself by applying a new solder alloy composition. But this also has a limitation since strengthening the solder joint can pose higher stress at the interface layer resulting in a crack free solder joint but a damaged dielectric at the package interface. Another approach is the enhancement of the total package or module, so that the stress per solder joint is reduced to a lower level, which is the use of underfill material. But even if it is a mature technology, the underfill process at the BGA board level component has a few challenges associated with no-clean flux residue, which can negatively impact the interface between the underfill material and the board interface, especially with larger WLCSP body size components. The re-workability of large underfilled components is also a factor, which needs to be thoroughly considered. Larger WLCSP components with fully underfilled configuration will be more difficult to be removed and re-worked. An alternative approach is a more localized enhancement using edgebond

materials with less volume adhesive. Since the outer array solder joints in WLCSP experience most of the damage accumulation during thermal cycling, an enhancement targeting those solder joints can result in a higher reliability and long-term thermal cycling performance. [4] But unlike smaller WLCSP with edgebond adhesive, the larger WLCSP are expected to behave different during thermal cycling with more thermo-mechanical fluctuation of the silicon wafer due to warpage. Implementing the edgebond on WLCSP components is expected to alter the shear fatigue mode and degradation mechanism due to the mitigation of the corner location strain, which usually caused by large CTE mismatch. To enable a more detailed and in-depth analysis, the grain structure development inside the solder joints were observed and signature microstructures are identified to understand the behavior of the interconnects on edgebond applied and thermal cycled components.

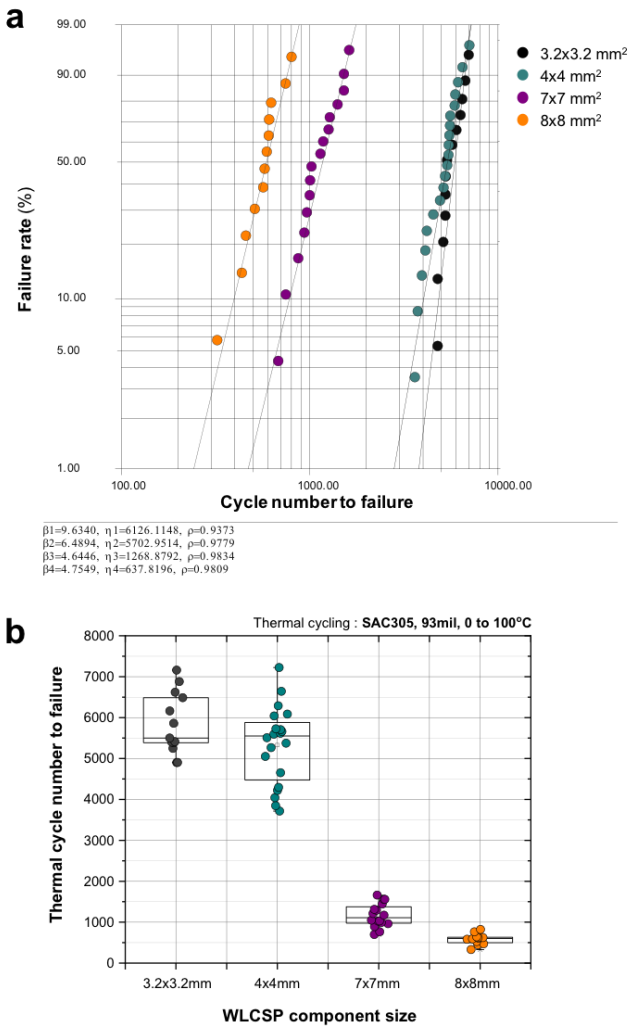

Figure 1. Weibull plot of 0 to 100ºC Thermal cycled WLCSP with various body sizes.

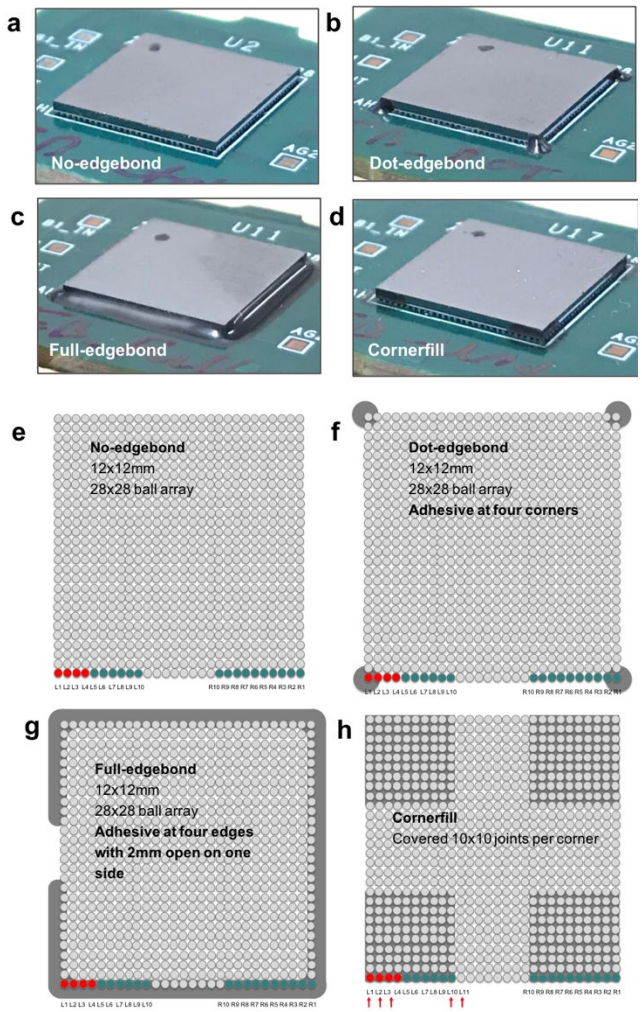

Figure 2. Edgebond sample component picture (a-d) and top view schematic configuration and ball array (e-h).

EXPERIMENTAL PROCEDURE

Body size of 12x12mm^2 with 0.4mm pitch, 250µm solder ball diameter WLCSP components were used in this study. Solder balls attached to the packages were all composed of Sn-4.0Ag-0.5Cu (wt%) (SAC405). The parts were board-assembled on 62mil high glass transition temperature (T_g), FR4-printed circuit boards with OSP surface finishes with a thermal profile of peak temperatures of 240 °C, 60 seconds above the liquidus temperature. All components were assembled with SAC305 solder paste. For edgebond process, commercially available reworkable edgebond adhesive were selected. A high T_g 130ºC and low CTE 30ppm/ºC reworkable edge-bond material was provided and processed by Zymet. The adhesive were applied to the WLCSP in three different configurations ; Dot-edgebond, Full-edgebond and Cornerfill. As shown in Figure 2(b,f), the Dot-edgebond is a configuration which has the four corner region with minimal adhesive applied. The penetration of the adhesive was minimal and only covered one solder joint at the corner. The Full-edgebond configuration is a configuration, which has all four edges with adhesive applied with a small opening of

2mm in one of the edge region. The penetration of the adhesive was also minimal and did not progress to the second row inside the component. Figure 2(d,h) presents the cornerfill configuration, a partial underfill configuration, which penetrated into the four corner region and covered 10x10 solder joint per corner. Figure 2(a)-(d) shows the actual picture of each configuration and Figure 2(e)-(h) shows the schematic top view and adhesive penetration per configuration. To prevent voiding due to moisture releasing from PCB material in curing cycle, test boards are pre-baked for 4 hours at 125°C after the adhesive was applied. The edgebond adhesives were dispensed at room temperature using a pneumatic, hand-held dispenser. The board was then cured at 150°C for 30 minutes. For thermal cycling, samples were cycled from -40 to 125 °C at a ramp rate of 10 °C per minute with 10 minutes of dwell time. A continuous resistivity measurement using a data logger was applied for each channel in situ monitoring during the test. The failure criterion in this study was based on the JESD22-A104D standard [5], a 20% increase of the peak resistivity for continuous five cycles relative to the initial value. The thermal cycling results for each condition were plotted as Weibull distribution plots. Cross-sectional analysis using optical microscope with bright light and polarized light and electro-backscattered diffraction (EBSD) imaging were applied to observe the evolution of the microstructures and the locations of the solder joint cracks.

RESULTS AND DISCUSSION

As shown in Figure 3 thermal cycling induce a degradation in the microstructure indicated as a grain refinement and grain recrystallization. Figure 3(a) shows the crack in a solder joint in the 12x12mm^2 WLCSP package corner after thermal cycling, in this case a selected joint after 400 cycles to failure. The associated electron backscattered diffraction (EBSD) inverse pole figure image in Figure 3(b) reveals the fine grain structure near the crack propagation path. These development structure is well explained with the development of sub-grain boundaries with low angle boundary evolution during thermal cycling, which is shown in Figure 4. [3] In earlier study, a series of 12x12mm^2 WLCSP were thermal cycled to segmented thermal cycling numbers and are subject to cross section to observe development of grain refinement, recrystallization and their correlation to the crack propagation. [6] Figure 5 shows the distribution of fine grained structure and the crack propagation path per solder joints, for five solder joints from each corner. TC0 indicates the initial state and TC400 indicates 400 thermal cycling. Beginning from the initial state cross section, an evolution of fine grain structure can be observed from the corner solder joints developing further into the inner solder joints once the cycle number reached 100.

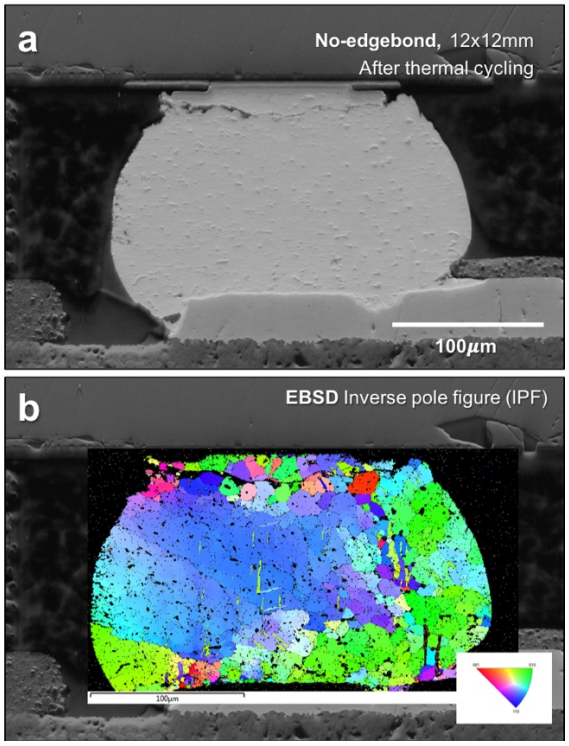

Figure 3. (a) SEM of 12x12mm^2 WLCSP package corner after thermal cycling to failure. (b) associated electron backscattered diffraction (EBSD) inverse pole figure image.

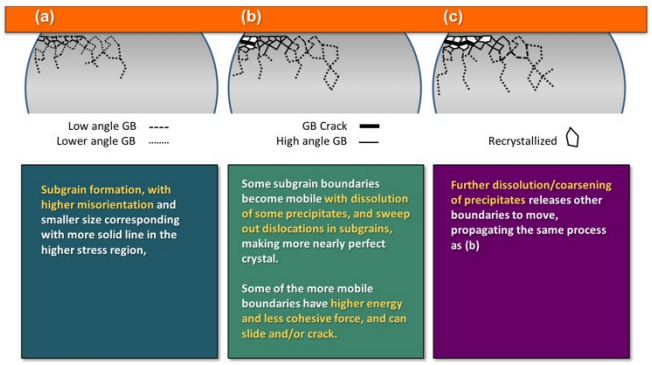

Figure 4. Crack initiation and propagation mechanism in solder joints during thermal cycling.[3]

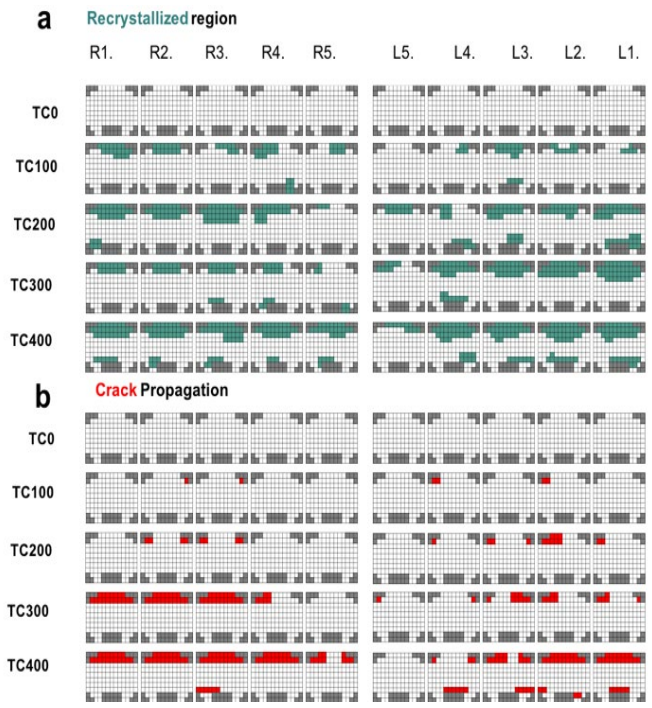

Figure 5. 12x12mm^2 WLCSP after segmented thermal cycling. (a) Recrystallization region and (b) Crack initiation and propagation path per solder joints after thermal cycling.

(Figure 5(a)) The associated crack location indicated per joints are shown in Figure 5(b). The crack developed also from the corner location solder joints at the package side interface then penetrated further with higher thermal cycling numbers to the inner solder joints. Given the fact that the damage accumulation with grain refinement and crack initiation are mostly from the corner solder joints, an enhancement focusing on the corner location seems to be an effective approach. Thus three different edgebond configurations were selected and applied. As already shown in Figure 2(b,f), the dot-edgebond configuration targeted the corner joints to be secured, compared to the full-edgebond configuration, which covered the four full edges but not penetrated into the component to ease the rework process. Having the adhesive only at the edge of the component also mitigated the interaction between the residual flux and the adhesive and did not cause any weak bonding at the PCB to adhesive interface. The weak interface between the residual flux and the adhesive is often a reason for a degraded thermal cycling performance, thus an adhesive avoiding the region where flux resides have a higher chance to avoid the complication. The thermal cycling results in a Weibull plot for the dot and full-edgebond configurations are presented in Figure 6(a), which are also compared to the baseline of no-edgebond applied samples. The components without any enhancement methods applied, showed a characteristic cycle number of around 311 cycles. As indicated in Figure 6(b), the no-edgebond applied components all failed around 300 cycles with a narrow data spread. But with edgebond applied, the characteristic life cycle number increased to 843 cycles and 3088 cycles, for dot-edgbeond and full-edgebond applied components, which is an increase of lifecycle time for 271% and 992% respectively. The main reason for this improvement in thermal cycling performance can be derived from the crack location map shown in Figure 7.

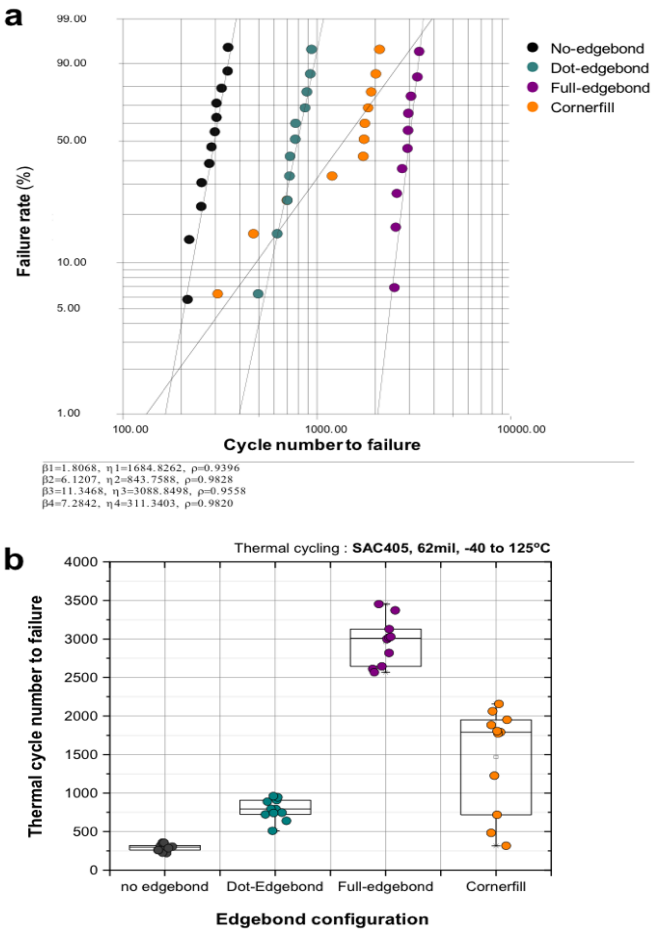

Figure 6. Thermal cycled WLCSP with no-edgebond, Dot-edgebond, full-edgebond and Cornerfill configuration. (a) Weibull and (b) failure cycle distribution plot.

The outermost rows were cross sectioned to reveal the solder joints and ten joints from the right and left side corners are presented in Figure 7. The location of the solder cross section regions are indicated in Figure 2(e-h). The crack propagated regions are indicated in red. Compared to the no-edgebond component, the dot-edgebond cross section revealed the two solder joints from each corner are crack free with crack propagation in the third solder joints. All of the crack propagation path were located at the package side interface. Four solder joints from the right side corner (R1-R4) are presented in Figure 8(b). Crack location paths are indicated with the white arrow. Compared to the dot-edgebond sample, the full-edgebond components show a crack propagation path

at the board side interface. Figure 8(c) show that the board side cracks are actually partial cracks inside the solder joint. Given the fact that these edge located solder joints, which are the outmost row solder joints, were covered with the adhesive, shear and tension of the solder joints are limited and show partial crack propagation instead of full cracks. The associated four solder joints form the right side corner (R1-R4) shown in Figure 8(c), which are indicated in Figure 2(g). Since the full-edgebond components were in the thermal cycling chamber for the longest among the three configurations, the Ag_3Sn intermetallic phase show the most accumulated size increase. The configuration which shows an intermediate improvement in thermal cycling performance was the cornerfill configuration shown in Figure 2(d,h). Unlike the dot-edgebond and full-edgebond configuration, the Cornerfill penetrated the component and covered 10x10 solder joints per corner, where the $12x12mm^2$ WLCSP has 28x28 solder ball array. The Weibull plot in Figure 6(a) for Cornerfill indicated characteristic lifecycle number of 1684 cycles or 540% improvement. Three of the sample though show an early failure compared to the general beta slope, which indicates a possibility of two failure modes. Further investigation is in process to find the root cause of the three relatively early failures, but the crack path at corner joints show a crack path at the board side interface (Figure 8(d)) revealing a possibility of a localized degradation mechanism, on corner joints which are not fully covered with the Cornerfill adhesive. The selected cross section in Figure 8(d) is the component which failed at the 482 cycles. A crack propagation path at the board side interface is observed with additional crack path at the package side interface in R1 and R3. To visualize the residual stress and lattice strain per solder joints, an EBSD analysis was performed and the resulted images are shown in Figure 9. Solder joints R1-R3 and R10,R11 from the Cornerfill component are presented. The location of the observed solder joints are indicated in red arrows in Figure 2(h). The inverse pole figure maps and the strain contour maps indicated that the right side of R1 retains a higher stress region compared to R2 and R3 solder joints. R10 also shows a higher stress intensity distribution, which is a solder joint located at the edge of the cornerfilled region. The outside edge of the cornerfill adhesive is indicated in red lines in Figure 9(a) and (d). R11 is the first solder joint outside the cornerfill region, which contains a wider opened crack at the upper right shoulder region. Based on these EBSD results, it seems that the corner location solder joints inside the cornerfill regions are in higher tension and residual stress, which is a direct indication of further fracture development, thus crack propagation.

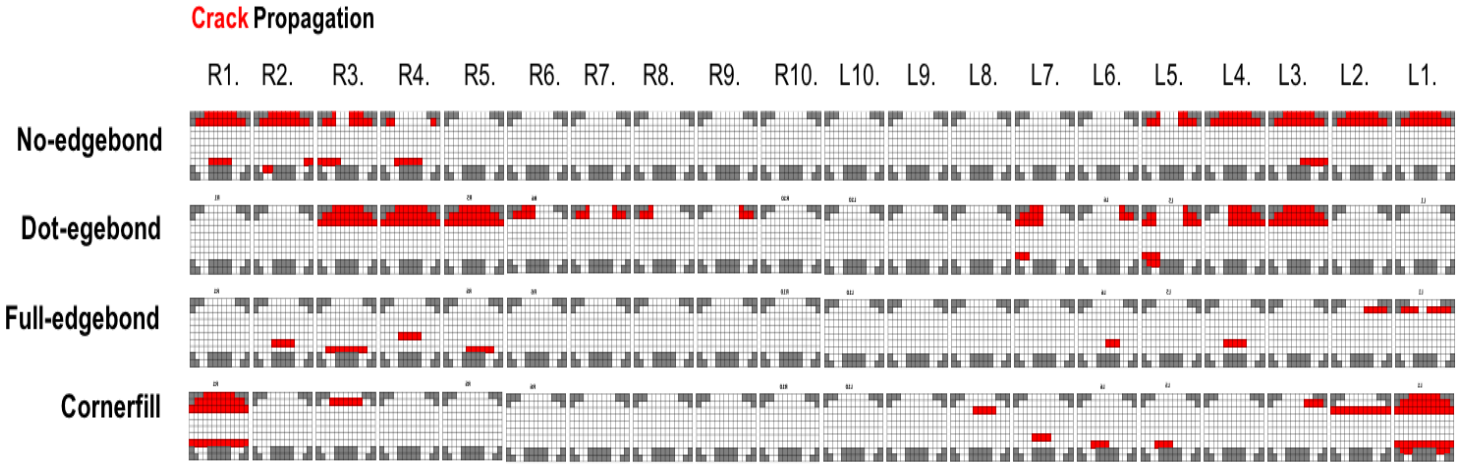

Figure 7. Thermal cycled WLCSP with no-edgebond, Dot-edgebond, full-edgebond and Cornerfill configuration. Crack propagation path indicated in red.

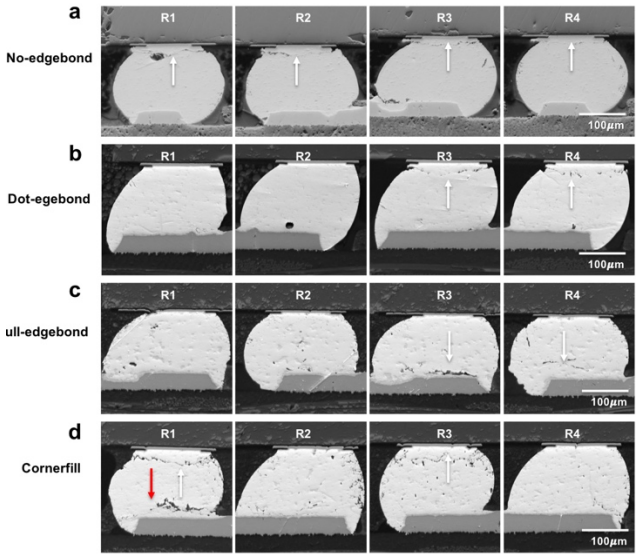

Figure 8. SEM images from R1 to R4 per edgebond configuration. (a) no-edgebond, (b) Dot-edgebond, (c) Full-edgebond and (d) Cornerfill solder joints. Location indicated in Figure 2(e-h).

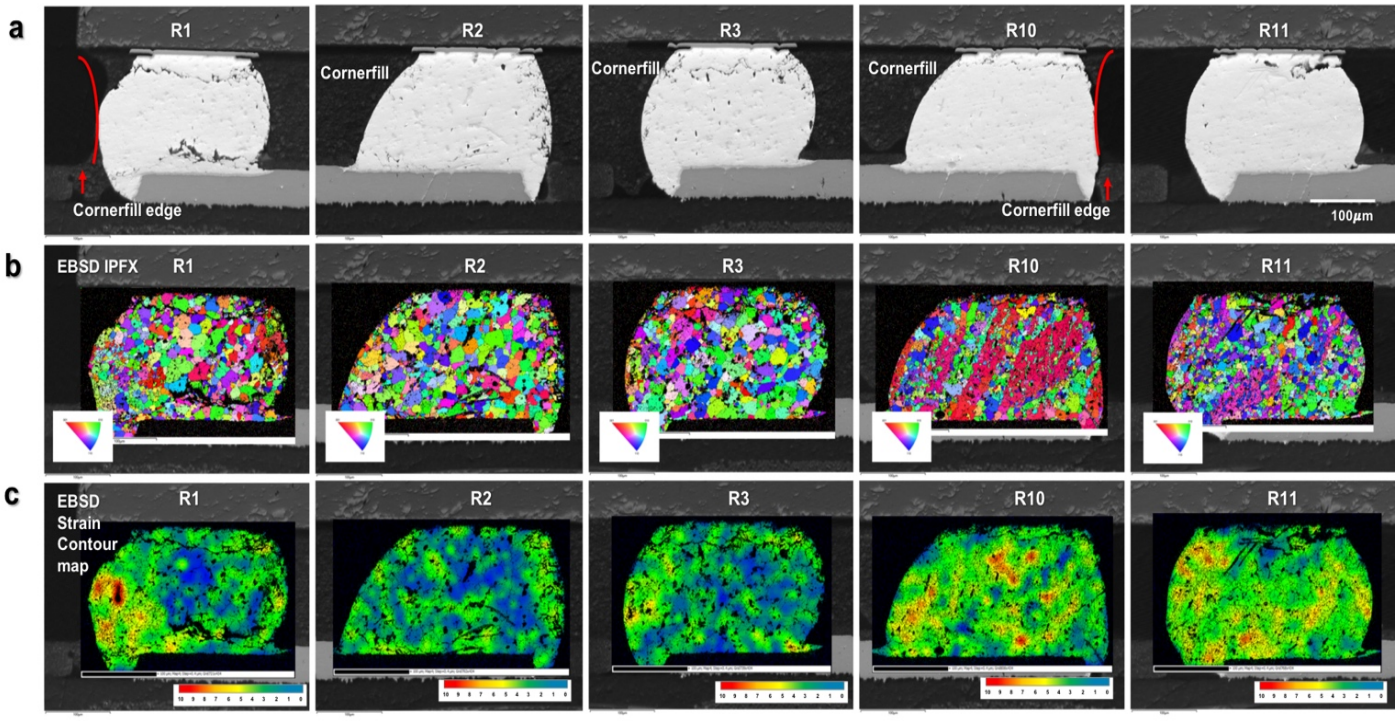

Figure 9. (a) SEM, (b) EBSD Inverse pole figure (IPF) image and (c) Strain contour map for Cornerfill component joint R1, R2, R3, R10 and R11. Redlines in (a) indicated the edge of the cornerfill region.

CONCLUSION

In this study, high stress 12x12mm^2 wafer level chip scale packages (WLCSP) were selected and subject to thermal cycling with full-edgebond, dot-edgebond and cornerfill adhesive, which improves the characteristic lifecycle numbers base on the configurations, but altered the failure location per configuration. The -40 to 125^{o}C thermal cycling revealed localized degradation per configuration during thermal cycling, showed a shift of the crack propagation path, based on full-edgebond, dot-edgebond and cornerfill adhesive sample conditions. But with edgebond applied, the characteristic life cycle number increased to 843 cycles and 3088 cycles, for dot-edgbeond and full-edgebond applied components, which is an increase of lifecycle time for 271% and 992% respectively. With Cornerfill application, a characteristic lifecycle number of 1684 cycles or 540% improvement was observed. The edgebond adhesive provided a vast increase of thermal cycling performance with minimal coverage. The EBSD analysis on edgebond covered and non-covered joints indicated a stress intensity distribution, that enables the visualization of the solder joints and indicated the joints, which are in higher chance of crack initiation and propagation.

ACKNOWLEDGEMENTS

This work is a research collaboration project supported by Zymet.

REFERENCES

1. J.W.Yoon, J.H.Bang, Y.H.Ko, S.H.Yoo, J.K.Kim and C.W.Lee, “Power Module Packaging Technology with Extended Reliability for Electric Vehicle Applications”, J. Microelectron. Packag. Soc., 21(4), 1-13 (2014).
2. S. Terashima, T. Kohno, A. Mizusawa, K. Arai, O. Okada, T. Wakabayashi, M. Tanaka, K. Tatsumi, “Improvement of Thermal Fatigue Properties of Sn-Ag-Cu Lead-Free Solder Interconnects on Casio's Wafer-Level Packages Based on Morphology and Grain Boundary Character”, Journal of Electronic Materials 38(1), 33-38 (2009)
3. Tae-Kyu Lee, Thomas Bieler, Choong-un Kim et al., “Fundamental of solder and interconnect technology”, Springer, Chapter 5, 132-133 (2014)
4. Andy Hsiao, Kola Akinade, Cherif Guirguis, Edward Ibe, Karl Loh and Tae-Kyu Lee, “The impact if conformal coating on WLCSP thermal cycle performance : Degradation mechanism and mitigation method”, Proceedings of SMTA International, September 17-21, Rosemont, IL, 745-750 (2017)
5. JEDEC Standard, JESD22-A104D, Thermal cycling, March 2009, http://www.jedec.org/standards-documents
6. Andy Hsiao, Mohamed Sheikh, Tony Crespo and Tae-Kyu Lee, “Compression and tension stress effect on WLCSP thermal cycling performance”, TMS2019, San Antonio, TX, March 11 (2019)